CLAIMS

What is claimed is:

1. A re-targetable communication processor, comprising:
   a. a connectivity unit;
   b. a digital signal processing core coupled to the connectivity unit;
   c. a plurality of scaleable functional units, coupled to the connectivity unit, to execute mathematically intensive operations, further including:
      a local memory;
      a plurality of removable complex arithmetic elements (hereinafter CAE) coupled to one another, to the local memory and to an inter-CAE bus; and
      a bus controller coupled to the inter-CAE bus and the connectivity unit.

2. The re-targetable communication processor according to claim 1, the CAE further comprising:
   a. a CAE memory to store data for the mathematically intensive operations;
   b. a sequencer, coupled to an arithmetic unit, a data router and the CAE memory, to generate addresses and control information;

c. the arithmetic unit, coupled to the CAE memory and the data router, optimized to execute operations in accordance with the control information; and

d. the data router to route data to the sequencer and the CAE memory and to facilitate communications among the CAEs in the scaleable functional unit.

3. The re-targetable communication processor according to claim 2, the CAE memory further comprising:

two banks of separately addressable data memories.

4. The re-targetable communication processor according to claim 3, the arithmetic unit further comprising:

a. a register file to accept data from the data memories; and

b. a plurality of multiplier-accumulator engines, coupled to one another, to the register file and to the data memories, to operate on the mathematically intensive operations.

5. The re-targetable communication processor according to claim 4, the multiplier-accumulator engine further comprising:

a. a pre-adder to generate a first sum by adding data from the register file and the data memory;

b. a multiplier to generate a multiplier output by multiplying data from the data memories or the first sum;

c. an accumulator to generate a second sum by adding the multiplier output or data from the data memories; and

d. a data packing block to configure the second sum into a pre-defined format.

6. The re-targetable communication processor according to claim 5, the multiplier further including a programmable shifter.

7. The re-targetable communication processor according to claim 1, the CAEs are coupled to one another via an east port, a west port and the inter-CAE port.

8. The re-targetable communication processor according to claim 1, further including a micro-controller core coupled to the connectivity unit.

9. The re-targetable communication processor according to claim 2, wherein a first delay introduced by the sequencer matches a second delay introduced by the arithmetic unit.

10. A scaleable functional unit in a re-targetable communication processor, comprising:

a. a local memory;

b. a plurality of removable complex arithmetic elements (hereinafter CAE) coupled to one another, to the local memory and to an inter-CAE bus; and

c. a bus controller coupled to the inter-CAE bus and the connectivity unit.

11. The scaleable functional unit according to claim 10, the CAE further comprising:

a. a CAE memory to store data for the mathematically intensive operations;

b. a sequencer, coupled to an arithmetic unit, a data router and the CAE memory, to generate addresses and control information;

c. the arithmetic unit, coupled to the CAE memory and the data router, optimized to execute operations in accordance with the control information; and

d. the data router to route data to the sequencer and the CAE memory and to facilitate communications among the CAEs in the scaleable functional unit.

12. The scaleable functional unit according to claim 11, the CAE memory further comprising:

two banks of separately addressable data memories.

13. The scaleable functional unit according to claim 12, the arithmetic unit further comprising:

a. a register file to accept data from the data memories; and

b. a plurality of multiplier-accumulator engines, coupled to one another, to the register file and to the data memories, to operate on the mathematically intensive operations.

14. The scaleable functional unit according to claim 13, the multiplier-accumulator engine further comprising:

a. a pre-adder to generate a first sum by adding data from the register file and the data memory;

b. a multiplier to generate a multiplier output by multiplying data from the data memories or the first sum;

c. an accumulator to generate a second sum by adding the multiplier output or data from the data memories; and

d. a data packing block to configure the second sum into a pre-defined format.

15. The scaleable functional unit according to claim 14, the multiplier further including a programmable shifter.

16. The scaleable functional unit according to claim 10, the CAEs are coupled to one another via an east port, a west port and the inter-CAE port.

17. The scaleable functional unit according to claim 11, wherein a first delay introduced by the sequencer matches a second delay introduced by the arithmetic unit.

18. A computer system, comprising:

a microprocessor coupled to a system bus;

a system controller coupled to the system bus; and

an input/output controller hub, coupled to the system controller and coupled to an input/output bus;

an add-in card, coupled to the input/output bus, further including:

a re-targetable communication system, comprising:

a. a connectivity unit;

b. a digital signal processing core coupled to the connectivity unit;

c. a plurality of scaleable functional units, coupled to the connectivity unit, to execute mathematically intensive operations, further including:

   i. a local memory;

   ii. a plurality of removable complex arithmetic elements (hereinafter CAE) coupled to one another, to the local memory and to an inter-CAE bus; and

   iii. a bus controller coupled to the inter-CAE bus and the connectivity unit.

19. The computer system according to claim 18, the CAE further comprising:

a. a CAE memory to store data for the mathematically intensive operations;

b. a sequencer, coupled to an arithmetic unit, a data router and the CAE memory, to generate addresses and control information;

c. the arithmetic unit, coupled to the CAE memory and the data router, optimized to execute operations in accordance to the control information; and

d. the data router to route data to the sequencer and the CAE memory and to facilitate communications among the CAEs in the scaleable functional unit.

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20. The computer system according to claim 19, the CAE memory further comprising:

two banks of separately addressable data memories.

21. The computer system according to claim 20, the arithmetic unit further comprising:

a. a register file to accept data from the data memories; and

b. a plurality of multiplier-accumulator engines, coupled to one another, to the register file and to the data memories, to operate on the mathematically intensive operations.

22. The computer system according to claim 21, the multiplier-accumulator engine further comprising:

a. a pre-adder to generate a first sum by adding data from the register file and the data memory;

b. a multiplier to generate a multiplier output by multiplying data from the data memories or the first sum;

c. an accumulator to generate a second sum by adding the multiplier output and data from the data memories; and

d. a data packing block to configure the second sum into a pre-defined format.

23. The computer system according to claim 22, the multiplier further including a programmable shifter.

24. The computer system according to claim 18, the CAEs are coupled to one another via an east port, a west port and the inter-CAE port.

25. The computer system according to claim 18, wherein the re-targetable communication system further including a micro-controller core that is coupled to the connectivity unit.

26. The computer system according to claim 19, wherein a first delay introduced by the sequencer matches a second delay introduced by the arithmetic unit.